



# Ivybridge Server Architecture: A Converged Server

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*Acknowledgments: Entire IVB Server Team*

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Available on select Intel® Core™ processors. Requires an Intel® HT Technology-enabled system. Consult your PC manufacturer. Performance will vary depending on the specific hardware and software used. For more information including details on which processors support HT Technology, visit <http://www.intel.com/info/hyperthreading>.

Requires a system with a 64-bit enabled processor, chipset, BIOS and software. Performance will vary depending on the specific hardware and software you use. Consult your PC manufacturer for more information. For more information, visit <http://www.intel.com/info/em64t>

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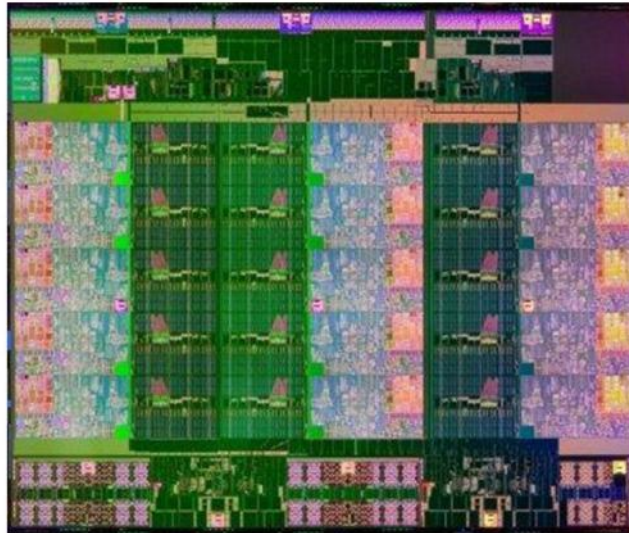
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# Ivytown: IvyBridge Server Processor

IvyBridge Server aka. IVT or IVB Server



Launched in August '13 and Feb'14 into two different server segments

- Up to 50% higher performance and energy efficiency over prior generation SandyBridge-E5 2Socket
- Up to 100% higher performance of prior generation Westmere-E7 4Socket

# Primary Product Goals

Cover wide spectrum of server portfolio with a converged architecture

Achieve scalable and energy efficient performance

Capitalize on the technology features of the Intel® 22nm process

# Covering the Server Space

## Server Space

- E5: Efficient Computing/Entry Level server  
WorkStation  
High-End-Desktops
- E7: Expandable / Mission Critical server

Historically supported via 2 product lines and 2 platforms

- Same core, 2 different uncore<sup>1</sup> designs
- E7 typically lagged E5 by ~1 year

## Challenges

- Overlap across the segment
- Fundamentally different segment requirements

E5	E7
1 socket	1 socket
2 sockets	2 sockets
4 sockets ring	4 sockets fully connected
	8 sockets

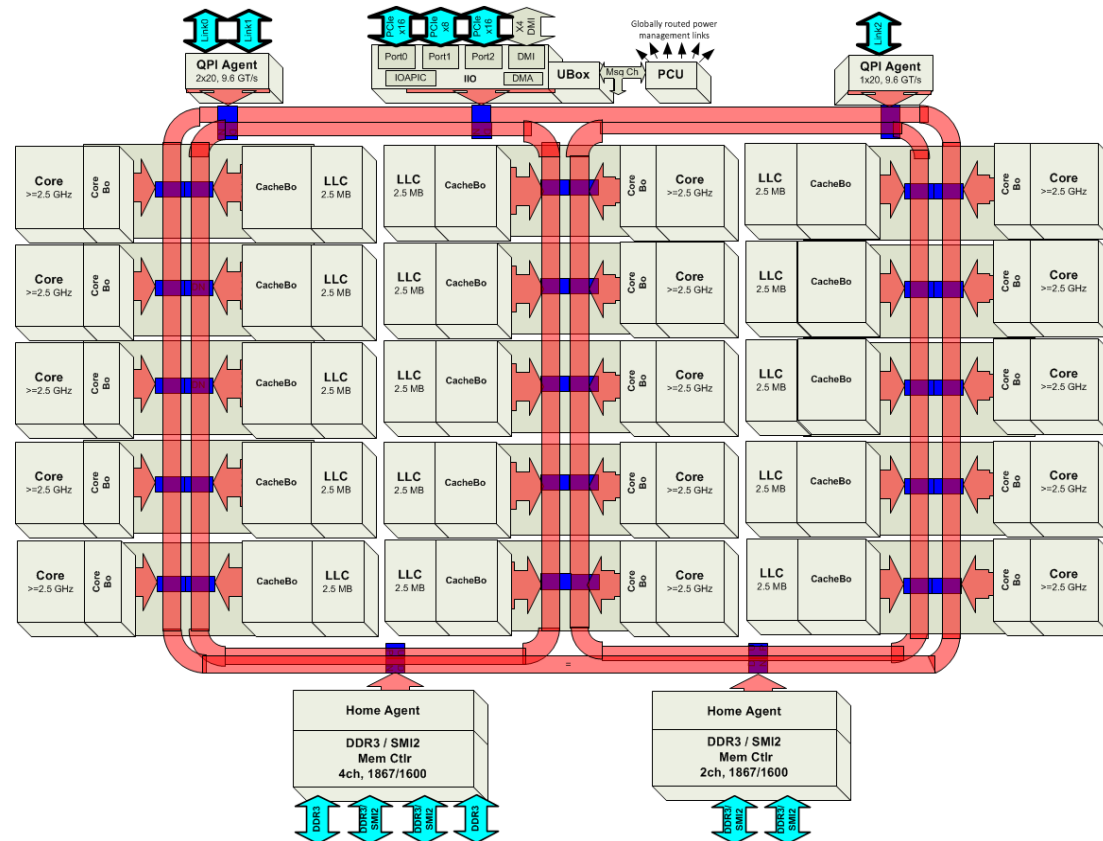
Supported Glue-less system socket counts

<sup>1</sup> Full chip is broken into core and uncore domains. Uncore is full chip except the cores.

# Converged Architecture

- Super set architecture
  - Glue-less 2/4/8 socket + Extensible Network Controller (XNC) support
  - 15 core/cache slices
  - 2 Memory Controllers
    - Both Native and Buffered memory
  - 2 Home Agents
  - 3 QPI links
  - 40 PCIe\* Gen3 lanes
  - Advanced RAS
- Configurability
  - Via chops (see next page)
  - Via feature Enabling/Disabling

## Micro-Architecture View



### Terminology reference:

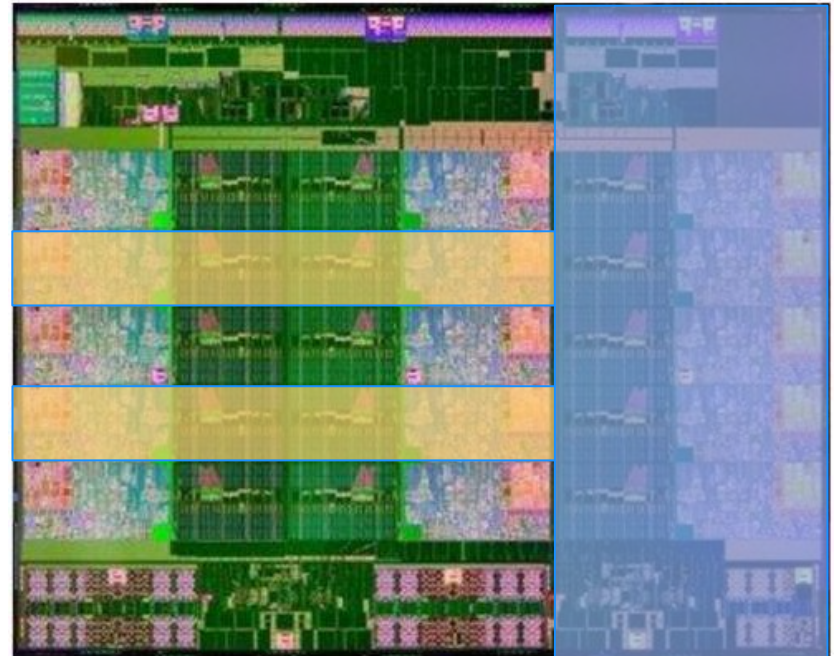
Ubox: Utility Box (global Uncore configuration Logic)  
CacheBo: Last Level Cache (LLC) Control Logic  
CoreBo: Core - Ring Interface Control Logic  
Cbo: CoreBo + CacheBo Logic  
PCU: Power Control Unit  
IIO: Integrated IO Unit

# Converged Architecture (cont.)

- Chop-able blocks

- Removal of right column
  - Cores/caches + agents on ring
- Removal of a row of cores/ caches

Floorplan View



Chop-able Column

Chop-able Rows



# Path to Performance

## Core improvement

- 5% increase in general compute IPC
- Specific ISA enhancements

## Socket performance features

- Up to 50% increase of cores & threads
- 25% - 50% increase in cache size and bandwidth
- 25% - 130% increase in memory bandwidth
- Efficient core performance scaling

## 22nm Process node

- Up to 30% system level performance per watt increase<sup>1</sup>
- Higher product frequencies

<sup>1</sup> Please refer to page 21 for details

Software and workloads used in performance tests may have been optimized for performance only on Intel® microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products.

# IVB Core

## Converged Core across Client and Server processors

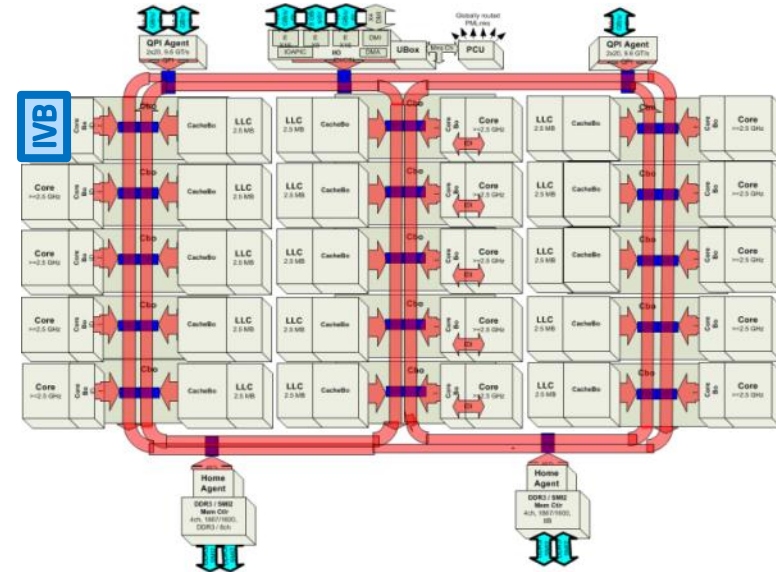
New for servers

Replaces SandyBridge and Westmere cores

5% general compute IPC increase

Recap of IVB Core Features

- ISA Additions
  - AVX (Advanced Vector eXtension) Float 16 conversion support
    - 16bit FP data support
  - Optimized REP MOVSB/STOSB <sup>1</sup>
  - Fast access of FS & GS base registers for user-threads
  - Intel® Secure Key - ISA Support for DRNG
  - Digital Random Number Generation instruction
  - Intel® OS Guard – Supervisor Mode Execution Protection
- Micro-architectural enhancements
  - MOV elimination<sup>2</sup>, pipelined divider
  - Next Page prefetcher
  - Shift/rotate and split-load features



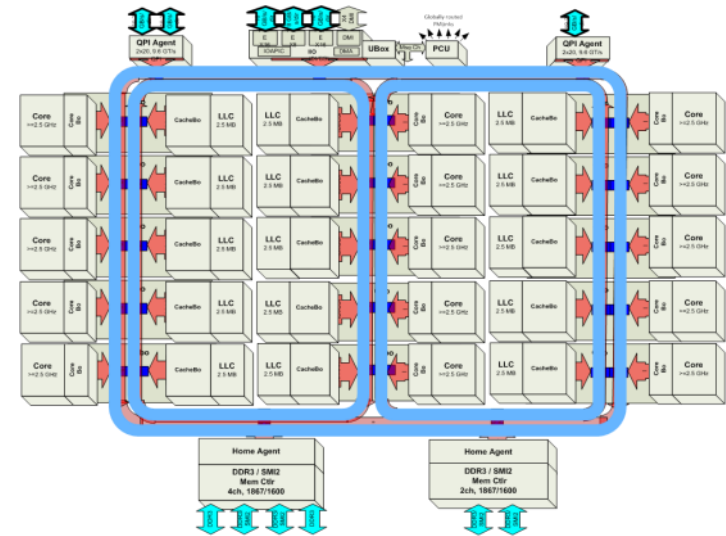
<sup>1</sup> Repeat Move Byte String, Store Byte String instructions

<sup>2</sup> Optimization to eliminate MOV pipeline occupancy

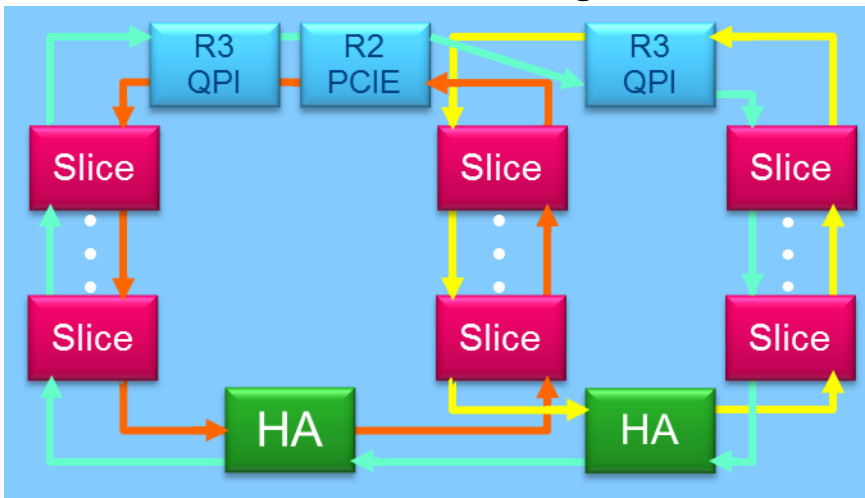
# Scalable On-die Interconnect

## Goal:

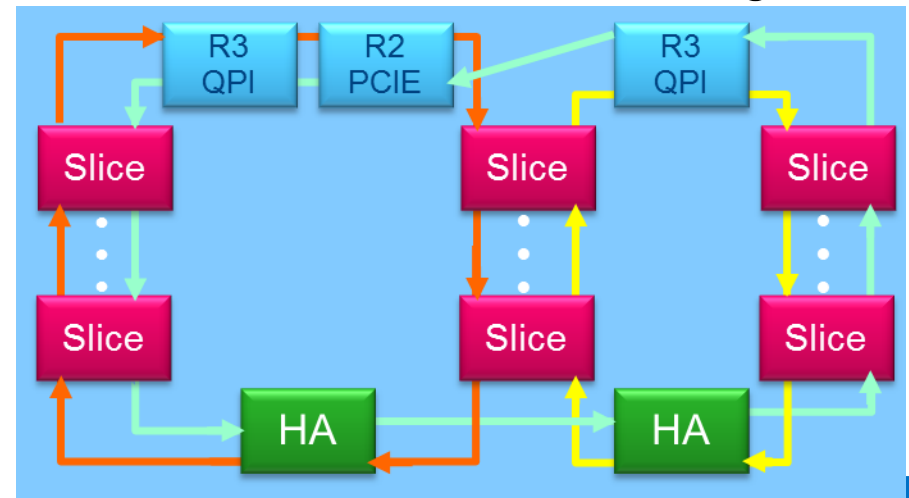
- Scalable ring performance
  - Keep latency and area increase in check
  - Improve performance
- 3 virtual rings
  - North/South switches dynamically configure the rings (as shown below)



## "Clockwise" Outer Ring



## "Counter-clockwise" Outer Ring



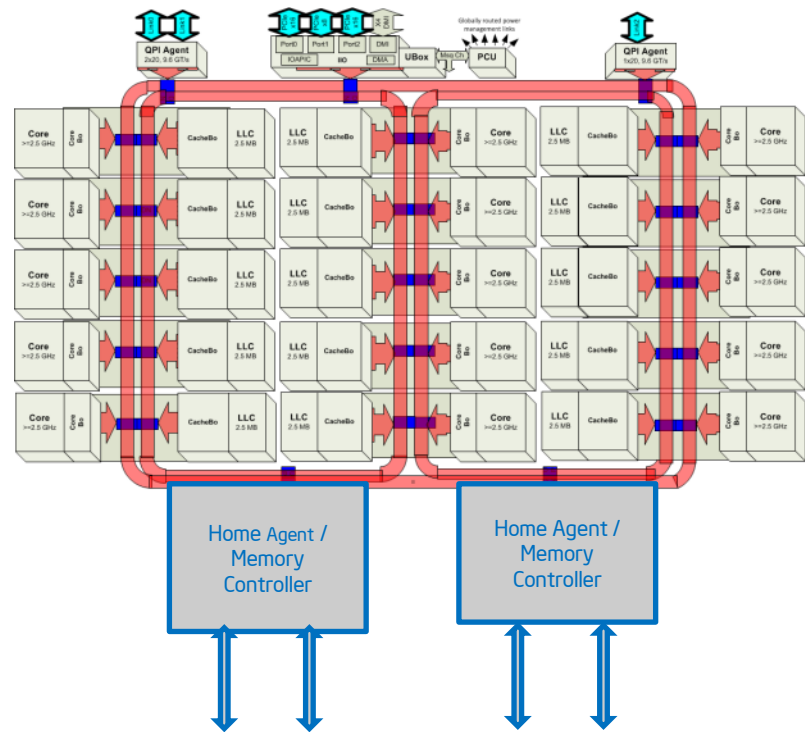
# Increased Memory Bandwidth and Socket Scalability

## Support higher memory speed

- Up to 1867 DDR3 speed

## Increased Memory scheduling efficiency

- Single/Dual Home Agent (HA) / Memory Controller (MC) with 4 DDR3 channels
- Deep buffering
  - 2 level tracker in HA
    - Large first level: Pre-allocated 512 entries
    - 128 entry second level
  - Increased Rd & Wr buffer sizes in MC
    - 48 Read Pending Queue entries per channel
    - 32 Write Pending Queue entries per channel
- MC Scheduler optimizations
  - Improved turnaround timings
  - Efficient Rd/Wr transaction mix scheduling



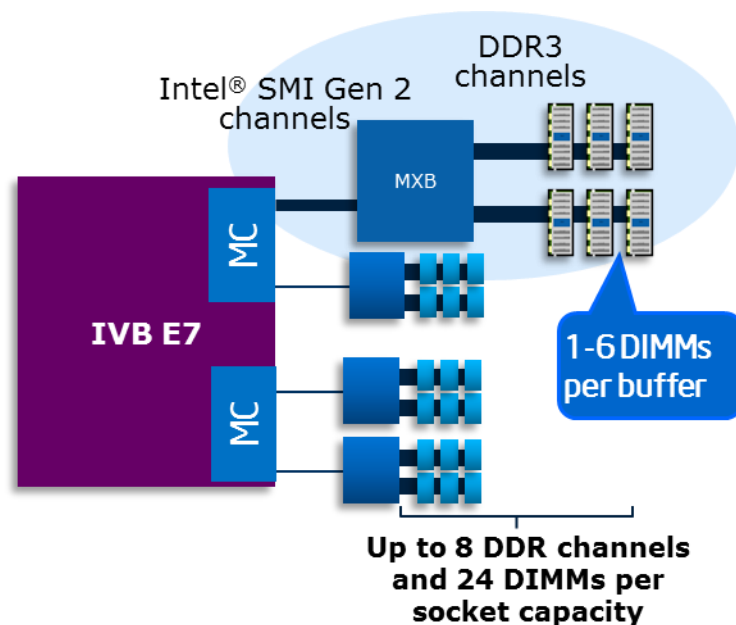
# Enable and Improve Buffered Memory Solution for E7

MC supports Scalable Memory Interface Gen2 in addition to DDR3

- Each SMI2 connects to a memory extension buffer (MXB)
- Each memory extension buffer connects to 2 DDR3 channels
- Up to 3 DIMMs per channel support

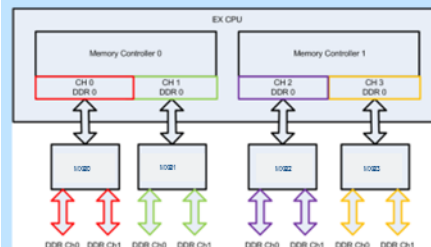
Two operation modes selectable in BIOS

- High reliability mode: Lock-step channels
  - DDDC support (Dual Device Data Correction)
- Performance mode: Independent channels
  - SDDC support (Single Device Data Correction)



## Lockstep Mode (1:1)

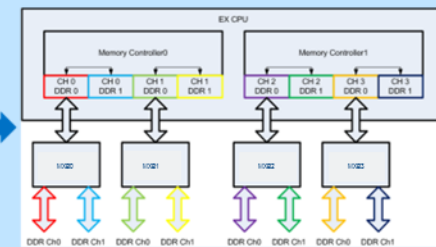
➤ Up to 1600 : 1600



1:1 SMI2 to DDR3 bus ratio  
DDR channels @ DDR3-1600  
SMI Gen 2 channels @ 1600

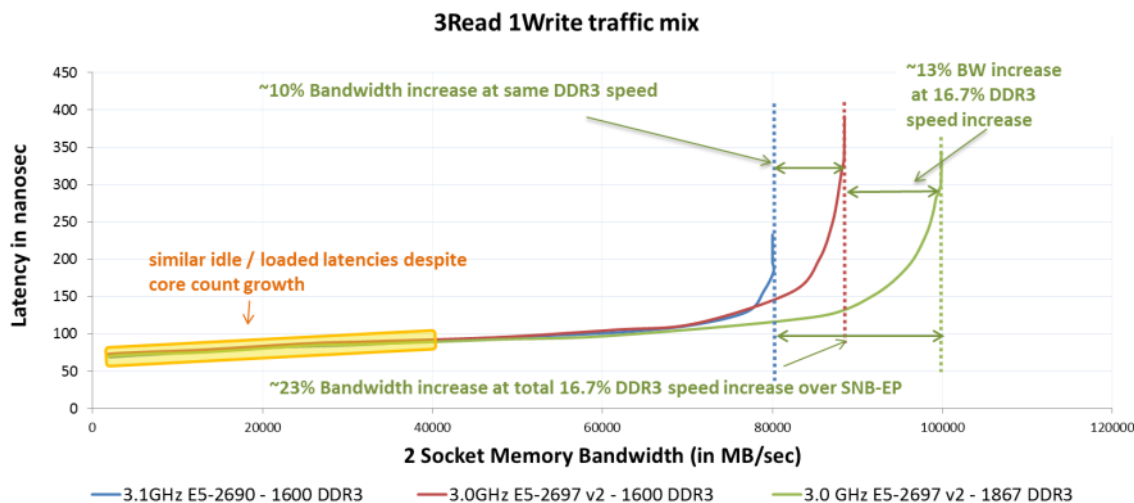
## Performance Mode (2:1)

➤ Up to 2667 : 1333

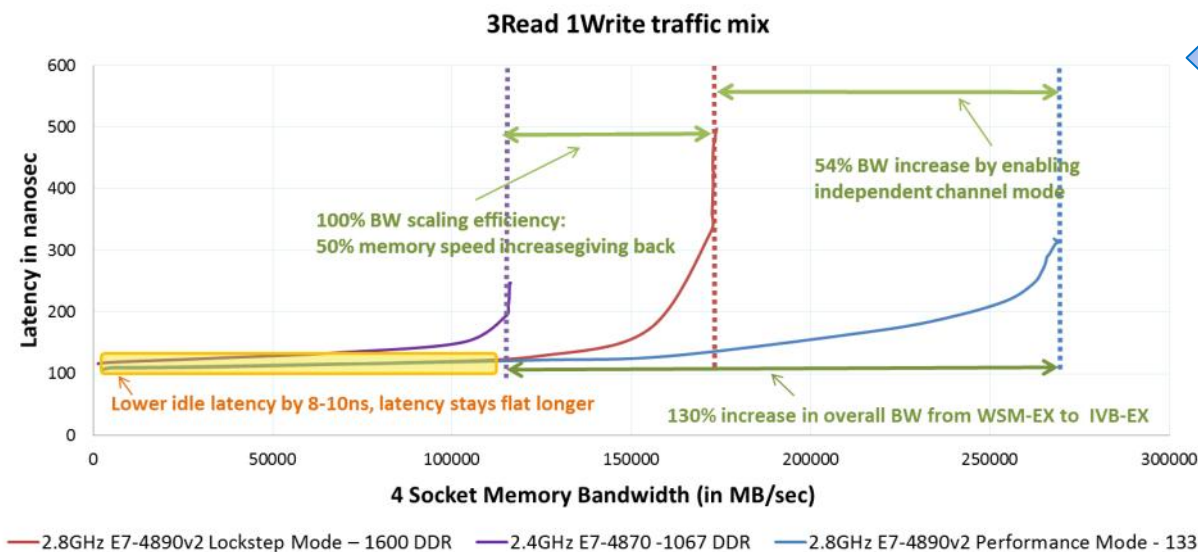


2:1 SMI2 to DDR3 bus ratio  
DDR channels @ DDR3-1333  
SMI Gen 2 channels @ 2667

# Resulting Memory Performance



← 2Socket E5 v2 local memory BW compared to prior generation



← 4Socket E7 v2 local memory BW compared to prior generation

*Increased Efficiency: Higher memory bandwidth increase compared to memory speed increase*

Intel® Xeon® Processor E5 2697 v2 and Intel® Xeon® Processor E7 4890 v2 memory bandwidth and latency results are compared to prior generation E5 and E7 products.

# Coherence Optimizations

Target to improve scalable system performance

Enabling the “in memory snoop directory” (aka. directory mode) for all systems

- Deprecated early snoop for 2 socket E5 systems
  - Improves load to use latencies for clean memory accesses
  - Removes snoop/snoop response processing from critical path

Going from 1bit to 2bit in memory directory

- Tracks 3 states – Invalid/Shared/Any
  - Eliminated need to snoop for Shared state memory accesses
  - Improves latency for Shared state accesses
  - Reduces snoop traffic

# New snoop mode to reduce directory overhead

## Opportunistic Snoop Broadcast (OSB)

- Speculative snoop broadcast prior to memory directory lookup
- Ignore snoop responses for Invalid/Shared directory state
- Improves cache latency

## Dynamically biased for power and performance

- OSB decision is based on available snoop bandwidth
- Usefulness of OSB is tracked to throttle or increase OSB

## Highly Configurable

- Enable/disable for different transaction types
- Adjustable thresholds to vary OSB rates for different transaction types



# IO Directory Cache (IODC) to reduce directory overhead

## Small cache in Home Agent (HA)

- 128 entries addressed by transaction id
- Used only for remote IO write transactions
- Supported only on glue-less system settings

## Functionality

- Entry allocated when the invalidation request (Invl2E) is received for a remote write transaction, along with snoop broadcast issue
- Entry de-allocated when the Write-Back data transaction is received by HA

## Saves

- The directory lookup and directory update for remote memory IO writes

# Improved IO Performance

## Large page support for IO Virtualization

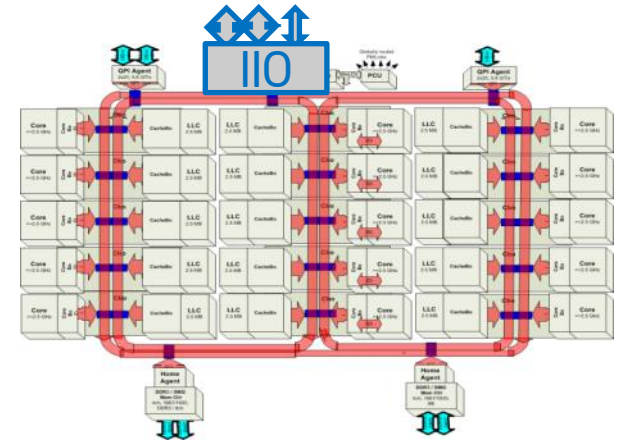
- 2MB and 1GB pages in Vt-d (Intel® Virtualization Technology for Directed I/O)
- Critical for small packet workloads with large working sets

## Arbitration optimizations for bandwidth

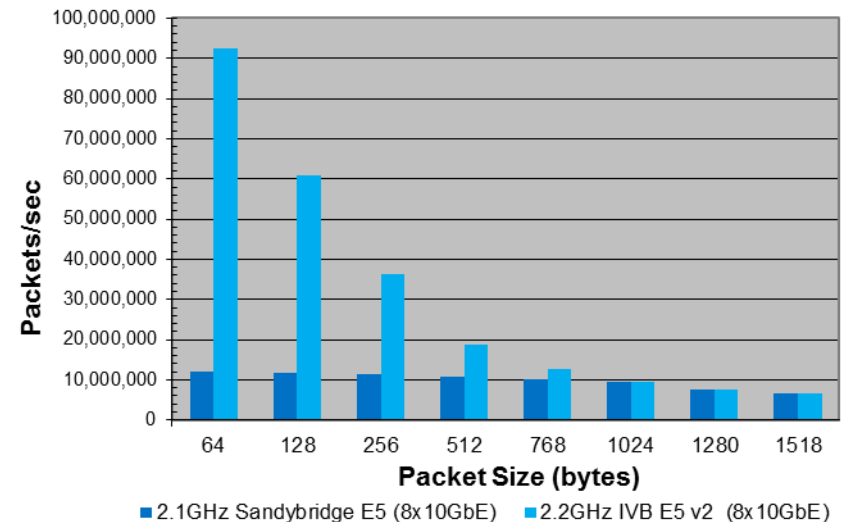
- Improved back to back scheduling
  - Higher PCIe\* Gen3 bandwidth
  - Increase in PCIe\* P2P (Peer2Peer) Bandwidth

## PCIe\* Atomics

- Read-Modify-Write transaction to/from IO



## Virtualized Packet Processing Performance



Results have been measured with intel® Data Plane Development Kit internally and are provided for informational purposes only. Any difference in system hardware or software design or configuration may affect actual performance.

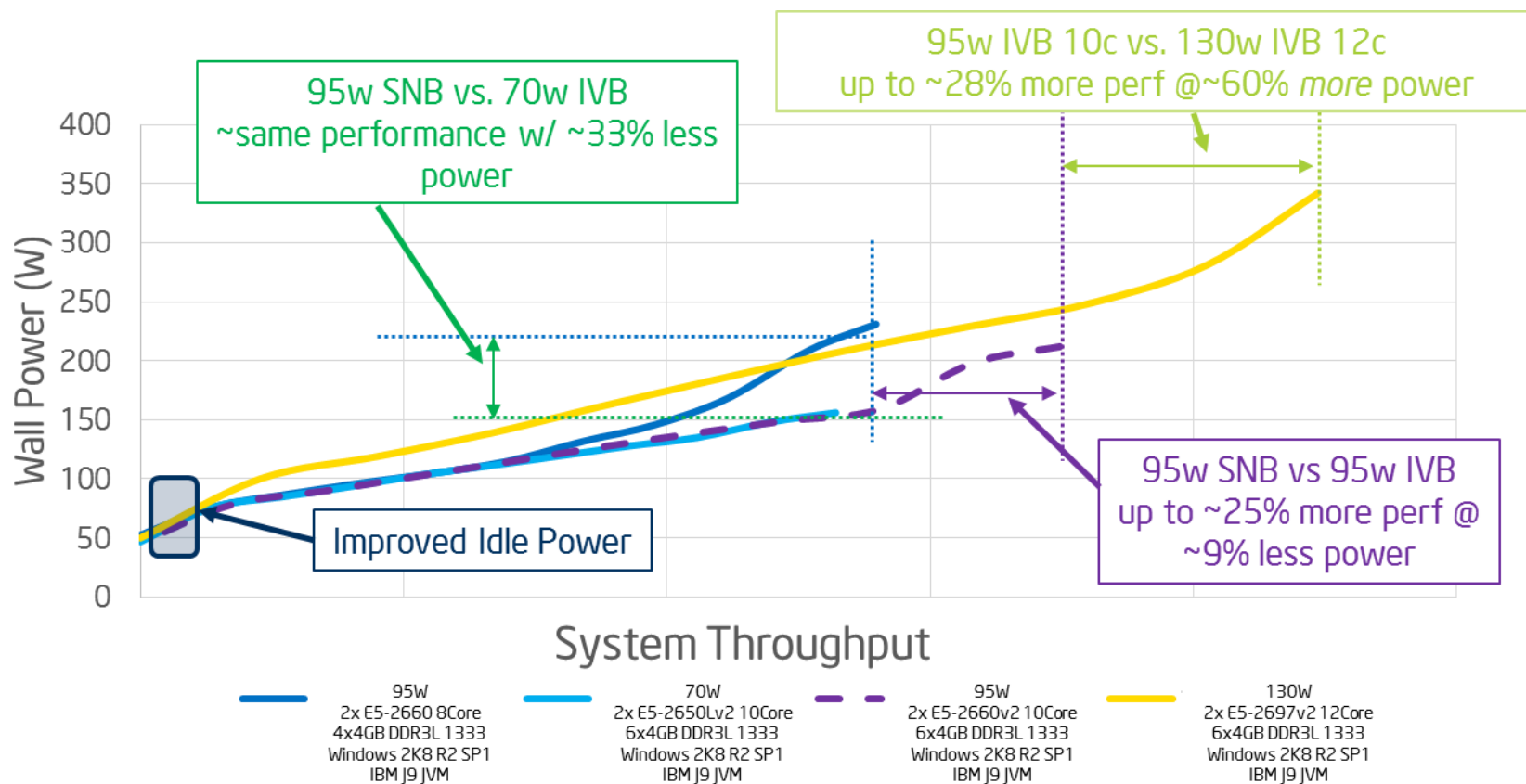
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# New Process: 22nm Process Technology

Improve power/performance

## Power Performance Load-line

Internal loadline benchmarking results



# Summary: A well balanced server processor

## Converged architecture covering the server space

- Refreshes E5 platforms
- Launches new E7 platforms
- 3 dies, 3 sockets, 75+ SKUs

## Focus on balanced and scalable system performance

- New Core and up to 50% more cores at increased frequency
- Up to 50% larger LLC capacity, great LLC throughput
- Major bandwidth improvements to keep the cores “fed”
- Increased CPU/memory frequency AND efficiency
- Improved IO BW

## Continued emphasis on power efficiency across the load-line

- With improved performance “when you need it”
- Focus on idle power and peak power/performance efficiency



# Backup

# References

## *Product briefs*

- <http://www.intel.com/content/dam/www/public/us/en/documents/product-briefs/xeon-e5-4600-v2-brief.pdf>
- <http://www.intel.com/content/dam/www/public/us/en/documents/product-briefs/xeon-e7-v2-family-brief.pdf>
- <http://www.intel.com/content/www/us/en/intelligent-systems/crystal-forest-server/xeon-e5-v2-89xx-chipset-ibd.html?wapkw=%22e5+v2%22+product+brief>

## *Data sheets*

- <http://www.intel.com/content/www/us/en/processors/xeon/xeon-e7-v2-datasheet-vol-1.html>
- <http://www.intel.com/content/www/us/en/processors/xeon/xeon-e7-v2-datasheet-vol-2.html>
- <http://www.intel.com/content/www/us/en/processors/xeon/xeon-e5-v2-datasheet-vol-1.html>
- <http://www.intel.com/content/www/us/en/processors/xeon/xeon-e5-v2-datasheet-vol-2.html>

## *Other manuals and specifications*

- <http://www.intel.com/content/www/us/en/intelligent-systems/romley/xeon-e5-2600-v2-series-appl-power-guide-addendum.html>
- <http://www.intel.com/content/www/us/en/processors/xeon/xeon-e5-2600-v2-uncore-manual.html>
- <http://www.intel.com/content/www/us/en/intelligent-systems/romley/xeon-e5-v2-c604-c602-j-chipset.html>
- <http://www.intel.com/content/www/us/en/processors/xeon/xeon-e5-v2-spec-update.html>
- Further product details and performance publications available through [www.intel.com](http://www.intel.com) and <http://ark.intel.com/>

# IVB Server products and platforms

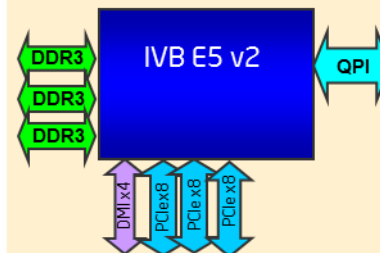
## E5 platform: Romley

- IVB Server - Romley platform refresh
  - E5 2600 - 1,2,4 sockets glueless and 2 socket scalable systems
  - E5 2400 - 1,2 sockets

## E7 platform: Brickland

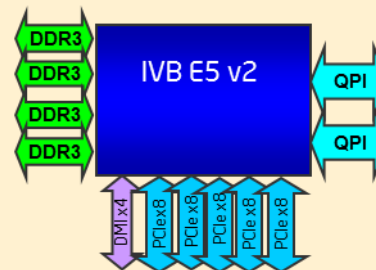
- New platform
  - 2, 4, 8 sockets glueless and 2, 4 socket scalable systems

**E5** entry level w/3 Native DDR3, 20 PCIe lanes, & 1 QPI link



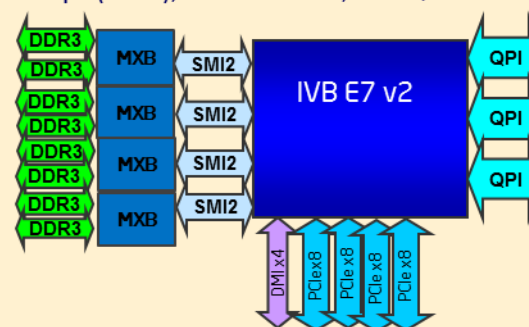
Socket B2

**E5** w/4 Native DDR3, 40 PCIe lanes, & 2 QPI links



Socket R

**E7** w/8 Native DDR3 through Memory eXtension Buffer chips (MXB), 32 PCIe lanes, & 2 QPI links

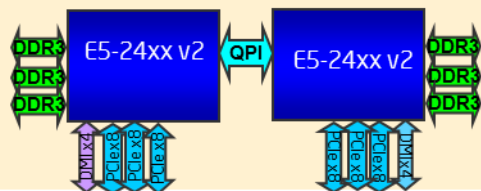


Socket R2

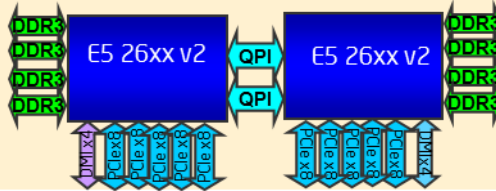
# IVB Server Products and Platforms

Romley: IVB Refresh Platform: 1, 2, 4 socket (S) glueless

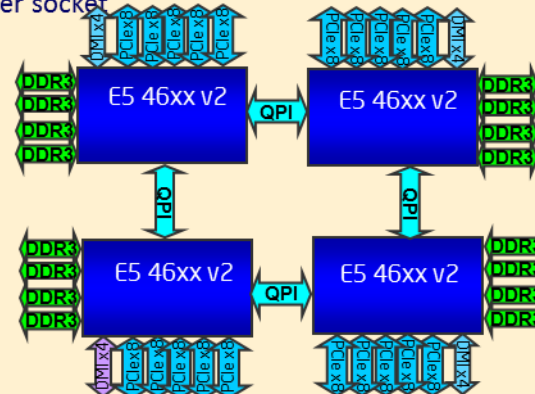
**E5 v2 2S** w/3 Native DDR3, 20 PCIe lanes, 1 QPI link per socket



**E5 v2 2S** w/4 Native DDR3, 40 PCIe lanes, 2 QPI links per socket

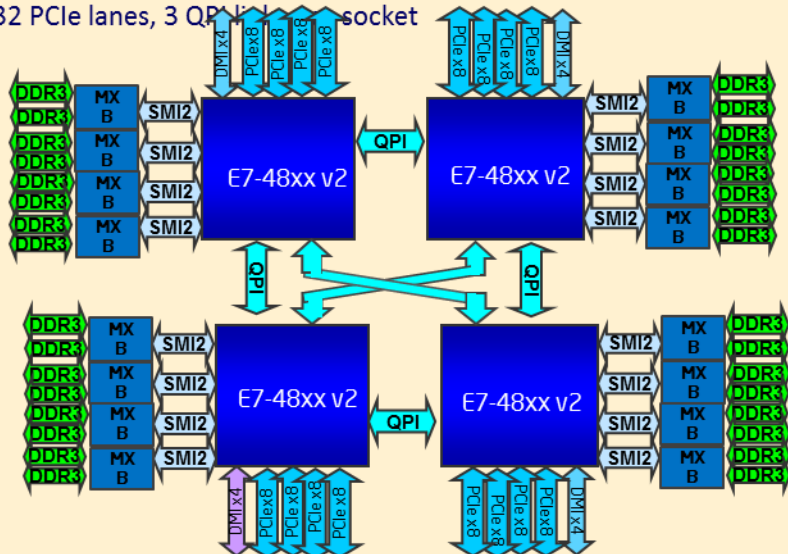


**E5 v2 4S** w/4 Native DDR3, 40 PCIe lanes, 2 QPI links per socket

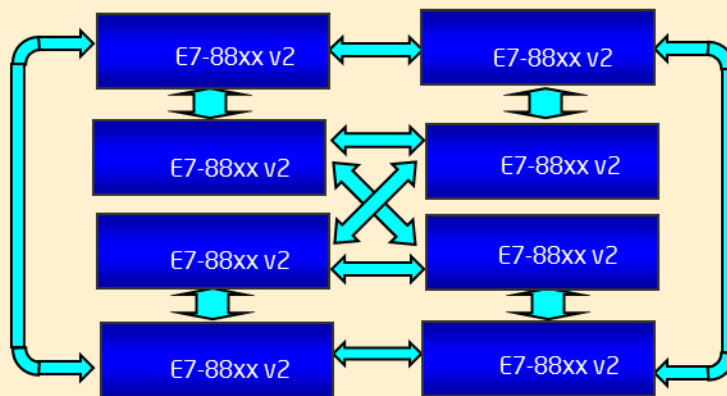


Brickland: New IVB EX Platform: 2, 4, 8 socket glueless

**E7 v2 4S** w/8 Native DDR3 through Memory eXtension Buffer chips (MXB)  
32 PCIe lanes, 3 QPI links per socket



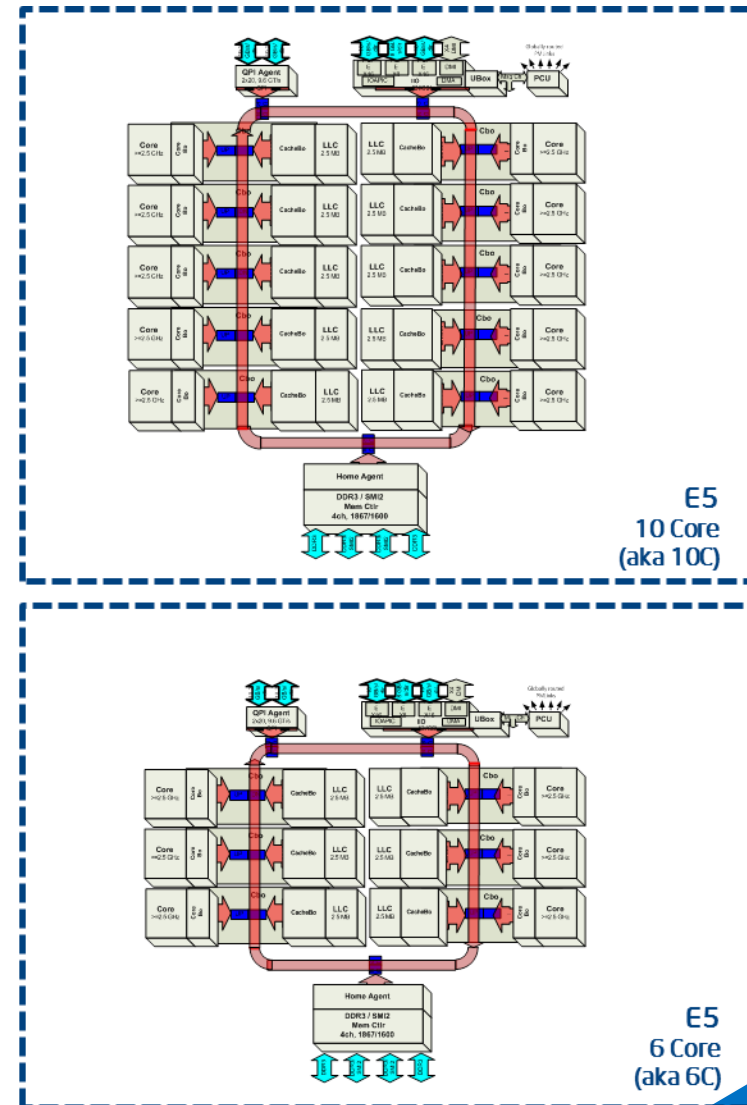
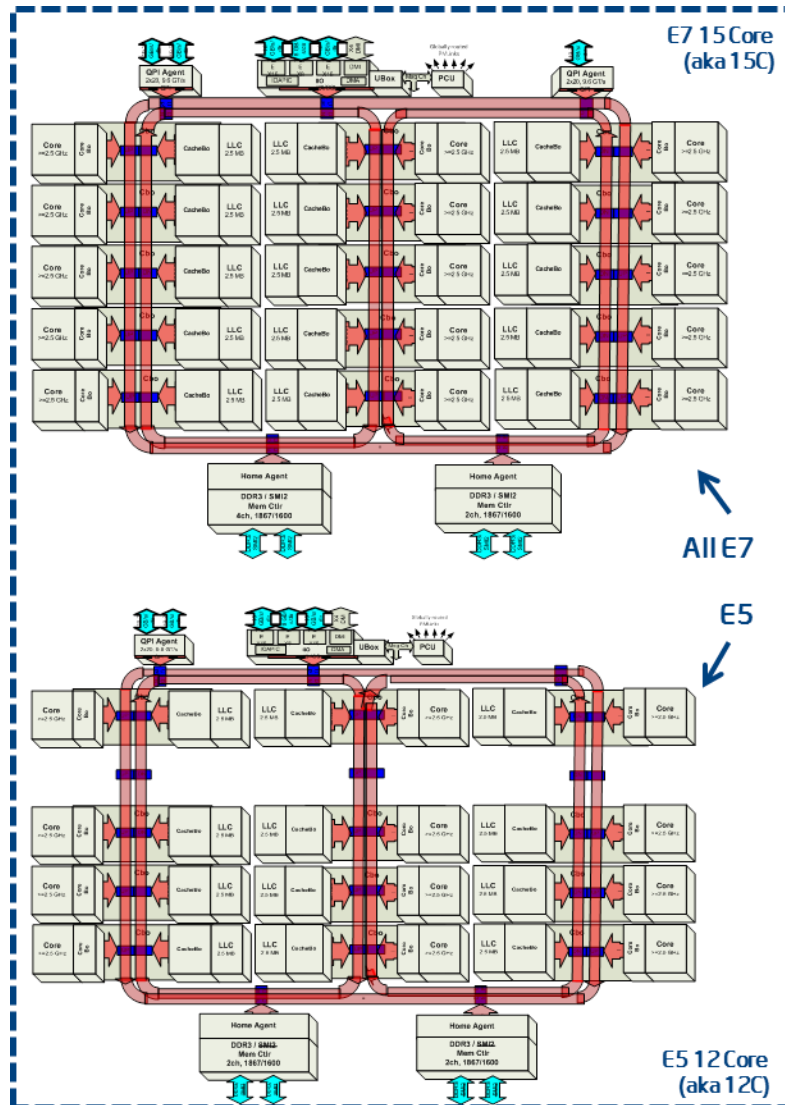
**E7 v2 8S** processors and QPI link connectivity shown only





# Total 3 IVB Server dies supply all IVB Server SKUs

One die for high core count E5 and all E7, one die each for mid and low core count E5 products



# IVB E5 Server Products

## Product names and specifications

### 2 Socket SKUs

Product Name	# of Cores	Max TDP Power	Last Level Cache Size	TDP Frequency
Intel® Xeon® Processor E5-2640 v2	8	95 W	20M	2GHz
Intel® Xeon® Processor E5-2643 v2	6	130 W	25M	3.5GHz
Intel® Xeon® Processor E5-2650 v2	8	95 W	20M	2.6GHz
Intel® Xeon® Processor E5-2650L v2	10	70 W	25M	1.7GHz
Intel® Xeon® Processor E5-2660 v2	10	95 W	25M	2.2GHz
Intel® Xeon® Processor E5-2667 v2	8	130 W	25M	3.3GHz
Intel® Xeon® Processor E5-2670 v2	10	115 W	25M	2.5GHz
Intel® Xeon® Processor E5-2680 v2	10	115 W	25M	2.8GHz
Intel® Xeon® Processor E5-2690 v2	10	130 W	25M	3GHz
Intel® Xeon® Processor E5-2695 v2	12	115 W	30M	2.4GHz
Intel® Xeon® Processor E5-2697 v2	12	130 W	30M	2.7GHz
Intel® Xeon® Processor E5-2609 v2	4	80 W	10M	2.5GHz
Intel® Xeon® Processor E5-2618L v2	6	50 W	15M	2GHz
Intel® Xeon® Processor E5-2620 v2	6	80 W	15M	2.1GHz
Intel® Xeon® Processor E5-2630 v2	6	80 W	15M	2.6GHz
Intel® Xeon® Processor E5-2630L v2	6	60 W	15M	2.4GHz
Intel® Xeon® Processor E5-2637 v2	4	130 W	15M	3.5GHz
Intel® Xeon® Processor E5-2603 v2	4	80 W	10M	1.8GHz
Intel® Xeon® Processor E5-2628L v2	8	70 W	20M	1.9GHz
Intel® Xeon® Processor E5-2648L v2	10	70 W	25M	1.9GHz
Intel® Xeon® Processor E5-2658 v2	10	95 W	25M	2.4GHz
Intel® Xeon® Processor E5-2687W v2	8	150 W	25M	3.4GHz

# IVB E5 Server Products (cont.)

## Product names and specifications

### 4 Socket SKUs

Product Name	# of Cores	Max TDP Power	Last Level Cache Size	TDP Frequency
Intel® Xeon® Processor E5-4610 v2	8	95 W	16M	2.3GHz
Intel® Xeon® Processor E5-4620 v2	8	95 W	20M	2.6GHz
Intel® Xeon® Processor E5-4627 v2	8	130 W	16M	3.3GHz
Intel® Xeon® Processor E5-4640 v2	10	95 W	20M	2.2GHz
Intel® Xeon® Processor E5-4650 v2	10	95 W	25M	2.4GHz
Intel® Xeon® Processor E5-4657L v2	12	115 W	30M	2.4GHz
Intel® Xeon® Processor E5-4603 v2	4	95 W	10M	2.2GHz
Intel® Xeon® Processor E5-4607 v2	6	95 W	15M	2.6GHz
Intel® Xeon® Processor E5-4624L v2	10	70 W	25M	1.9GHz

### 1 Socket Server, Workstation SKUs

Product Name	# of Cores	Max TDP Power	Last Level Cache Size	TDP Frequency
Intel® Xeon® Processor E5-1660 v2	6	130 W	15M	3.7GHz
Intel® Xeon® Processor E5-1650 v2	6	130 W	12M	3.5GHz
Intel® Xeon® Processor E5-1620 v2	4	130 W	10M	3.7GHz

# IVB E5 Entry Level Server Products

## Product names and specifications

### 2 Socket SKUs

Product Name	# of Cores	Max TDP Power	Last Level Cache Size	TDP Frequency
Intel® Xeon® Processor E5-2440 v2	8	95 W	20M	1.9GHz
Intel® Xeon® Processor E5-2450 v2	8	95 W	20M	2.5GHz
Intel® Xeon® Processor E5-2450L v2	10	60 W	25M	1.7GHz
Intel® Xeon® Processor E5-2470 v2	10	95 W	25M	2.4GHz
Intel® Xeon® Processor E5-2407 v2	4	80 W	10M	2.4GHz
Intel® Xeon® Processor E5-2418L v2	6	50 W	15M	2GHz
Intel® Xeon® Processor E5-2420 v2	6	80 W	15M	2.2GHz
Intel® Xeon® Processor E5-2430 v2	6	80 W	15M	2.5GHz
Intel® Xeon® Processor E5-2430L v2	6	60 W	15M	2.4GHz
Intel® Xeon® Processor E5-2448L v2	10	70 W	25M	1.8GHz
Intel® Xeon® Processor E5-2428L v2	8	60 W	20M	1.8GHz
Intel® Xeon® Processor E5-2403 v2	4	80 W	10M	1.8GHz

### 1 Socket SKUs

Product Name	# of Cores	Max TDP Power	Last Level Cache Size	TDP Frequency
Intel® Xeon® Processor E5-1428L v2	6	60 W	15M	2.2GHz

# IVB E7 Server Products

## Product names and specifications

### 2, 4 and 8 Socket Scalable SKUs

Product Name	# of Cores	Max TDP Power	Last Level Cache Size	TDP Frequency
Intel® Xeon® Processor E7-8893 v2	6	155 W	37.5M	3.4GHz
Intel® Xeon® Processor E7-8891 v2	10	155 W	37.5M	3.2GHz
Intel® Xeon® Processor E7-8890 v2	15	155 W	37.5M	2.8GHz
Intel® Xeon® Processor E7-8880L v2	15	105 W	37.5M	2.2GHz
Intel® Xeon® Processor E7-8880 v2	15	130 W	37.5M	2.5GHz
Intel® Xeon® Processor E7-8870 v2	15	130 W	30M	2.3GHz
Intel® Xeon® Processor E7-8857 v2	12	130 W	30M	3GHz
Intel® Xeon® Processor E7-8850 v2	12	105 W	24M	2.3GHz
Intel® Xeon® Processor E7-4890 v2	15	155 W	37.5M	2.8GHz
Intel® Xeon® Processor E7-4880 v2	15	130 W	37.5M	2.5GHz
Intel® Xeon® Processor E7-4870 v2	15	130 W	30M	2.3GHz
Intel® Xeon® Processor E7-4860 v2	12	130 W	30M	2.6GHz
Intel® Xeon® Processor E7-4850 v2	12	105 W	24M	2.3GHz
Intel® Xeon® Processor E7-4830 v2	10	105 W	20M	2.2GHz
Intel® Xeon® Processor E7-4820 v2	8	105 W	16M	2GHz
Intel® Xeon® Processor E7-4809 v2	6	105 W	12M	1.9GHz
Intel® Xeon® Processor E7-2890 v2	15	155 W	37.5M	2.8GHz
Intel® Xeon® Processor E7-2880 v2	15	130 W	37.5M	2.5GHz
Intel® Xeon® Processor E7-2870 v2	15	130 W	30M	2.3GHz
Intel® Xeon® Processor E7-2850 v2	12	105 W	24M	2.3GHz